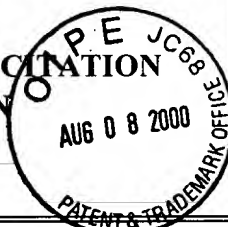


Form PTO-1449

**INFORMATION DISCLOSURE CITATION
IN AN APPLICATION**

(Use several sheets if necessary)

ATTY DOCKET NO.
1247-0428PAPPLICATION NO.
09/593,945APPLICANT
Hitoshi NAOEFILING DATE
June 15, 2000GROUP
Not Assigned
U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
GM	5,887,040	3/23/99	Jung et al.			
mm	5,237,290	8/17/93	Banu et al.			

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION	
						YES	NO
GM	6-53950	2/25/94	JAPAN			PART.	
gm	7-193562	7/28/95	JAPAN			PART.	
mm	9-181713	7/11/97	JAPAN			PART.	
AM	10-247903	9/14/98	JAPAN			PART.	
GM	9-36849	2/7/97	JAPAN			PART.	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	GM	"Phase-Locked Loops-Design, Simulation, and Applications", Roland E. Best, <u>The Classical Digital PLL (DPLL)</u> , pp. 156-163, 1997.
	mm	"A CMOS Serial Link for Fully Duplexed Data Communication", Kyeongho Lee et al., <u>IEEE Journal of Solid-State Circuits</u> , Vol. 30, No. 4, pp. 353-364, April 1995.

EXAMINER

DATE CONSIDERED

November 7, 2003

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

DJD:kna

[illegible]